#13

Docket No.: YHK-0065 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of:

Seong Cheol SHIN

Serial No. 09/836,204 : Group Art Unit: 2673

Confirm. No. 6497 : Examiner: Lun Yi Lao

Filed: April 18, 2001 : Customer No.: 34610

For: METHOD AND APPARATUS FOR DRIVING PLASMA DISPLAY PANEL UTILIZING ASYMMETRY SUSTAINING

TRANSMITTAL OF APPEAL BRIEF

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window, Mail Stop Appeal Brief-Patents
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed December 29, 2003. Enclosed is Check No.11567 for the Appeal Brief fee of $330.00.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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Sir:

This appeal is taken from the final rejection of claims 1-12 as set forth in the final Office Action of August 28, 2003 (hereinafter the Office Action). In accordance with 37 CFR §1.192, applicant addresses the following items.

REAL PARTY IN INTEREST

The real party in interest is LG Electronics Inc.

RELATED APPEALS AND INTERFERENCES

The Applicant is unaware of any related appeals or interferences.

STATUS OF THE CLAIMS

Claims 1-12 have been finally rejected and are on appeal.

STATUS OF AMENDMENTS

A Second Amendment After Final Rejection is being filed simultaneously with this Appeal Brief to cancel claims 13-14, 16-19 and 21-22 (without prejudice or disclaimer). The Amendment After Final Rejection filed on November 25, 2003 was entered, as indicted in the Advisory Action dated December 8, 2003. The claims on appeal (after entry of the Second Amendment After Final Rejection) are in the attached Appendix.

SUMMARY OF THE INVENTION

The present specification describes a structure and operation of a plasma display panel (PDP). As shown in Figure 1, a discharge cell of a three electrode, AC surface discharge PDP includes a scanning/sustaining electrode 12Y and a common sustaining electrode 12Z formed on an upper substrate 10, and an address electrode 20X formed on a lower substrate 18. See page 1, line 23-page 2, line 4 of the present specification. Figure 2 shows a PDP 30 adopting a block division system that is divided into an upper block 38 and a lower block 40. A discharge cell 1 is provided at each intersection among the scanning/sustaining electrode lines Y1 to Ym, common sustaining electrode lines Z1 to Zm and address electrode lines X11 to X1n and X21 to X2n. See page 2, lines 23-31.

The driving of such a PDP 30 may require a high voltage of more than hundreds of volts. Accordingly, a driving circuit of the PDP 30 may include an energy recovery circuit to reduce a power consumption of the PDP 30. See page 4, lines 22-28.

In one discussed arrangement, an external sustaining voltage Xsusup is applied to the energy recovery circuit after a rising edge enable signal XE/Rup was applied thereto. When the rising-edge enable signal is applied to the energy recovery circuit, a voltage charged in the source capacitor may be applied to the address electrode lines X11 to X1n and X21 to X2n. Then driving signals XTop and XBottom of the address drivers 36A and 36B is raised into a sustaining level (i.e., a stabilizing level prior to application of the external sustaining voltage Xsusup). See page 6, line 14-page 7, line 1. As discussed at page 7 beginning on line 21, video data and clock signals are applied in a period at which the driving signals XTop and XBottom of the address drivers 36A and 36B are stabilized and thereby a scanning interval is lengthened.

Fig. 5 shows a plasma display panel (PDP) 60 divided into an upper block 56 and a lower block 58. A driving apparatus includes a first scanning/sustaining driver 50A connected to the scanning/sustaining electrode lines Y1 to Ym/2 in the upper block 56, a second scanning/sustaining driver 50B connected to the scanning/sustaining electrode lines Ym/2+1 to Ym in the lower block 58, a common sustaining driver 52 connected to the common sustaining electrode lines Z1 to Zm, a first address driver 54A connected to the address electrode lines X11 to X1n in the upper block 56, a second address driver 54B connected to the address electrode lines X21 to X2n in the lower block 58, and a controller 62 for controlling the first and second drivers 54A and 54B. See page 11, lines 8-20. The first and second scanning/sustaining drivers

50A and 50B apply a scanning pulse and a sustaining pulse to the scanning/sustaining electrode lines Y1 to Ym in the upper and lower blocks 56 and 58. The first and second address drivers 54A and 54B apply a data pulse synchronized with the scanning pulse to the address electrode lines X11 to X1n and X21 to X2n in the upper and lower blocks 56 and 58. The common sustaining driver 52 applies a sustaining pulse to all the common sustaining electrode lines Z1 to Zm included in the upper/lower blocks 56 and 58. See page 11, line 31-page 12, line 8.

Embodiments of the present invention may apply the driving signal XTop in the upper block 56 and the driving signal XBottom in the lower block 58 in such a manner to overlap with each other. That is, the driving signal XBottom at the lower block 58 may be applied at a half time of an application period of the driving signal XTop at the upper block 56. See page 14, line 25-page 15, line 3; and page 12, lines 14-18; and Fig. 6. Since a period when the driving signals for the upper and lower blocks are changed to overlap with the period when the driving signals for the other corresponding blocks are stabilized, the scanning interval can be reduced. See page 16, lines 4-10.

Embodiments of the present invention relate to high speed driving of a plasma display. The scanning interval can be reduced by driving two sets of address electrodes in an asymmetrical fashion. The shortened scan interval allows for higher speed driving of the plasma display device which may result in a higher quality image.

ISSUES ON APPEAL

Whether each of claims 1-12 is unpatentable under 35 U.S.C. §103(a) over U.S. Patent 5,995,069 to Tokunaga et al. (hereafter Tujunga) in view of U.S. Patent 6,229,516 to Kim et al. (hereafter Kim).

GROUPING OF THE CLAIMS

Each of claims 1-12 stands or falls separately from one another.

ARGUMENT

The present application includes two independent claims, namely claim 1 and claim 9. These claims contain different features as may be evidenced by the specifically claimed features and as may be pointed out below. For ease of illustration, similar types of claims (or claim features) may be discussed with respect to each other. This is not an admission that the claims are the same or that the stand or fall together. Rather, this is an attempt to narrow the number of issues and to limit the number of arguments. While arguments may be similar for different claims, it should be understood that differently claimed features are expressly used.

The Office Action rejects claims 1-12 under 35 U.S.C. §103(a) over Tokunaga in view of Kim. As will be described below, applicant respectfully submits that the combination of Tokunaga and Kim is improper and/or that if the combination is made, the combination also does not teach or suggest the claimed features.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation in the references themselves to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success for the modification or combination of references. The teaching or suggestion to make the modification or combination of prior art and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). There must be particular findings as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge to the claimed invention to combine or modify references. *In re Kotzab*, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir. 2000). Conclusory statements cannot be relied up for particular combinations of prior art and specific claims. *In re Lee* 277 F.3d 1338, 61U.S.P.Q.2d 1430 (Fed. Cir. 2002).

Independent claim 1 recites a method of driving a plasma display panel utilizing an asymmetry sustaining wherein the plasma display panel is divided into an upper block and a lower block for its driving. The method includes applying an upper driving signal for supplying a data to address electrode lines provided at the upper block, and applying a lower driving signal for supplying a data to address electrode lines provided at the lower block in such a manner to overlap with the upper driving signal.

As one example, the present specification shows a plasma display array having an upper block 56 and a lower block 58. The upper block 56 may be driven by a first address driver 54A

and the lower block 58 may be driven by a second address driver 54B. As shown in Figure 6, the driving signal XTop of the upper block 56 may be driven in such a manner to overlap with the driving signal XBottom of the lower block 58.

The Office Action asserts that Tokunaga teaches a method for driving a plasma display including applying upper driving signals (D1-D12) to address electrode lines provided at an upper block and applying lower driving signals (D1-D12) to address electrode lines provided at a lower block. See Tokunaga's Figure 11. The Office Action asserts that Tokunaga fails to drive a plasma display panel utilizing asymmetrical sustaining.

The Office Action then relies on Kim as teaching an asymmetrical driving method for driving a flat panel display. However, Kim relates to a driving technique of a liquid crystal display (LCD) panel. That is, Kim's Figure 2 specifically shows an LCD having data drivers 12, 14 and gate drivers 22, 24. The driving technique of a LCD is different than a driving method for plasma display panels. The Office Action appears to suggest that because Kim discloses a flat panel display, that the driving methodologies for a liquid crystal display can be applied to a plasma display. That is, the Office Action asserts that is would have been obvious to modify Tokunaga with the teaching of Kim such that the drivers of Tokunaga would be independently operated to perform an asymmetrical driving method. However, there is no basis for this assertion. Rather, the driving methodologies for a liquid crystal display and a plasma display panel are different from one another.

For example, Tokunaga discloses that a data electrode driver 101 applies a pixel data pulse to each of data electrodes D1-Dn for driving the data electrode. The Y-row electrode

driver 102 produces a reset pulse forcibly exciting the discharge between the Y-row electrodes, thereby producing a reset pulse for generating charged particles in the discharge space, priming pulse for reproducing the charged particle, scanning pulse for writing the pixel data, sustaining pulse for sustaining the discharge and emission of light, and erasing pulse for erasing the charge. These pulses are applied to the row electrodes corresponding to the input timing pulses for driving the Y-row electrodes. See col. 5, lines 25-40. The X-row electrode driver 103 produces the reset pulse for forcibly exciting the discharge of the X-row electrodes for producing charged particles in the discharge space, and a sustaining pulse for sustaining the discharge and emission of light. The pulses are applied to the row electrodes corresponding to input timing pulses for driving the Y-row electrodes. See col. 5, lines 40-49.

In stark contrast, Kim's liquid crystal display includes a plurality of pixels. Each pixel has a pixel electrode, a storage capacitor and a switching element (such as a thin film transistor). See Figures 4 and 5 for example. The switching element may be turned on or off responding to the scanning signal from a gate line and the switching element transmits the image signal from the data line to the pixel electrode in its on state. See col. 4, line 59-col. 5, line 15. Kim applies gate signals to a switching element (such as a transistor) so as to transmit image signals. This differs significantly from the signals applied by Tokunaga's data electrode driver 101, Y-row electrode driver 102 and X-row electrode driver 103. Merely because Kim discloses gate line signals applied at different times, this does not suggest that the drivers of a plasma display may be modified as suggested in the Office Action. As such, there is no suggestion to make the

combination as alleged in the Office Action. There is no suggestion in the applied references for asymmetrically driving a plasma display panel.

Additionally, the Office Action references Kim's col. 8, lines 6-19 and Fig. 9 to show an asymmetry driving method. A start signal STV1 is applied to driver 22 and a start signal STV2 is applied to driver 24 to begin to apply upper and lower data A to the corresponding pixels. See col. 8, lines 20-28. There is no suggestion of how Tokunaga's plasma display panel may be modified such that data is output by data drivers 34a and 34b based on start signals (such as Kim's STV1 and STV2). Tokunaga operates upon a different driving methodology and may not be modified as suggested in the Office Action. The mere assertion in the Office Action that this modification may be made is insufficient to show the obviousness of the alleged combination.

Still further, the Office action asserts (on page 6) that Kim does [not] disclose a plasma display panel utilizing asymmetry (at Figures 2, 9 and column 1, lines 10-18). This is not true. Kim's col. 1, lines 10-18 does mention plasma display panels as being used for computer monitors. There is no indication that plasma display panels utilize asymmetry as stated in the Office Action.

A *prima facie* case of obviousness has not been established because neither Tokunaga nor Kim teaches or suggests a plasma display panel utilizing asymmetry sustaining. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Further, there is no particular findings in either Tokunaga nor Kim as to specific understandings and principles within the knowledge of a skilled artisan that would have motivated one to modify or combine either Tokunaga or Kim to teach or suggest a plasma display panel utilizing asymmetry sustaining. *In re Kotzab*, 217 F.3d 1365, 55

U.S.P.Q.2d 1313 (Fed. Cir. 2000). At least for these reasons, a *prima facie* case of obviousness has not been established. Independent claim 1 therefore defines patentable subject matter.

Independent claim 9 recites a driving apparatus for a plasma display panel utilizing an asymmetry sustaining wherein the plasma display panel is divided into an upper block and a lower block. The driving apparatus includes a first address driver for driving first address electrode lines included in the upper block and a second address driver for driving second address electrode lines included in the lower block. Control means are also included for applying first and second control signals having a desired phase difference to each of the first and second address drivers.

For at least the reasons set forth above, Tokunaga and Kim may not be combined as alleged to find all the features of independent claim 9. Even if combined, the references still do not suggest all the features of independent claim 9. That is, the references do not suggest the claimed phase difference to each of the first and second address drivers.The Office Action also asserts that Kim teaches a controller 100. However, Kim's controller 100 does not apply first and second control signals having a desired phase difference to each of the first and second address drivers. The asserted combination therefore does not teach or suggest all the features recited in independent claim 9.

Dependent claim 2 recites that the lower driving signal is applied at an approximately halftime of an application period of the upper driving signal. The Office Action references Kim's liquid crystal display as teaching these features. However, Kim does not relate to a driving signal applied at approximately halftime of an application period of the upper driving signal of a

plasma display panel. Signals produced in Kim's liquid crystal display do not relate to driving signals of a plasma display panel. The asserted combination therefore does not teach or suggest all the features of dependent claim 2, especially in combination with the other features of independent claim 1.

Dependent claim 3 recites a period when a period when the upper driving signal falls into a ground potential overlaps with a period when the lower driving signal remains at a stable voltage level. Kim does not suggest these features as alleged in the Office Action. The asserted combination therefore does not teach or suggest all the features of dependent claim 3, especially in combination with the other features of independent claim 1.

Dependent claim 4 recites a period when the lower driving signal falls into a ground potential overlaps with a period when the upper driving signal remains at a stable voltage level. Kim does not suggest these features as alleged in the Office Action. The asserted combination therefore does not teach or suggest all the features of dependent claim 4, especially in combination with the other features of independent claim 1.

Dependent claim 5 recites a data at the lower block is supplied at said period when the lower driving signal remains at a stable voltage level. Kim does not suggest these features as alleged in the Office Action. The asserted combination therefore does not teach or suggest all the features of dependent claim 5, especially in combination with the other features of independent claim 1.

Dependent claim 6 recites a data at the upper block is supplied at said period when the upper driving signal remains at a stable voltage level. Kim does not suggest these features as

alleged in the Office Action. The asserted combination therefore does not teach or suggest all the features of dependent claim 6, especially in combination with the other features of independent claim 1.

Dependent claim 7 recites driving an energy recovery circuit at the application time of the driving signals to raise the driving signals into a stable voltage level, and driving the energy recovery circuit after the data was supplied to the corresponding block, thereby falling the driving signals into a ground voltage level. The Office Action never addresses these claimed features relating to driving an energy recovery circuitry and therefore the Office Action fails to make a *prima facie* case of obviousness. There is no suggestion for the claimed driving of an energy recovery circuit as recited in claim 7, especially in combination with the other features of independent claim 1.

Dependent claim 8 recites signals for driving the energy recovery circuit have a phase difference between the upper block and the lower block. The Office Action never addresses these claimed features relating to driving the energy recovery circuit and therefore the Office Action fails to make a *prima facie* case of obviousness. There is no suggestion for the claimed driving of an energy recovery circuit as recited in claim 8, especially in combination with the other features of independent claim 1.

Dependent claim 10 recites the control means includes controller for generating the first and second control signals and applying them to the first and second address drivers, and a delay, being provided between the controller and the second address driver, for delaying the second control signal. The Office Action asserts that Kim teaches a controller 100. However,

Kim's controller 100 does not generate the claimed first and second control signals or the claimed delay provided between the controller and the second address driver for delaying the second control signal. The asserted combination therefore does not teach or suggest all the features of dependent claim 10, especially in combination with the other features of independent claim 9.

Dependent claim 11 recites the delay delays the second control signal such that a driving signal can be applied from the second address driver to the address electrode lines at an approximately half time of a driving signal applied from the first address driver to the address electrode lines. The Office Action references Kim as teaching these claimed features of dependent claim 11. However, Kim does not relate to a driving signal applied from the first address driver to the address electrode lines. The asserted combination therefore does not teach or suggest all the features of dependent claim 11, especially in combination with the other features of independent claim 9.

Dependent claim 12 recites a first scanning/sustaining driver for driving scanning/sustaining electrode lines included in the upper block, a second scanning/sustaining driver for driving scanning/sustaining electrode lines included in the lower block, and a common sustaining driver for driving common sustaining electrode lines included in the upper and lower blocks. Tokunaga does not teach or suggest these features as alleged in the Office Action. The asserted combination therefore does not teach or suggest all the features of dependent claim 12, especially in combination with the other features of independent claim 9.

CONCLUSION

It is respectfully submitted that the above arguments show that each of claims 1-12 are patentable over the applied references. Based at least on these reasons, it is respectfully submitted that each of claims 1-12 defines patentable subject matter. Applicant respectfully requests that the rejections of claims 1-12 set forth in the August 28 Office Action be withdrawn.

Respectfully submitted,
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APPENDIX

1. , A method of driving a plasma display panel utilizing an asymmetry sustaining wherein the plasma display panel is divided into an upper block and a lower block for it's driving, said method comprising the steps of:

applying an upper driving signal for supplying a data to address electrode lines provided at the upper block; and

applying a lower driving signal for supplying a data to address electrode lines provided at the lower block in such a manner to overlap with the upper driving signal.

2. The method as claimed in claim 1, wherein the lower driving signal is applied at an approximately halftime of an application period of the upper driving signal.

3. The method as claimed in claim 1, wherein a period when a period when the upper driving signal falls into a ground potential overlaps with a period when the lower driving signal remains at a stable voltage level.

4. The method as claimed in claim 1, wherein a period when the lower driving signal falls into a ground potential overlaps with a period when the upper driving signal remains at a stable voltage level.

5. The method as claimed in claim 3, wherein a data at the lower block is supplied at said period when the lower driving signal remains at a stable voltage level.

6. The method as claimed in claim 4, wherein a data at the upper block is supplied at said period when the upper driving signal remains at a stable voltage level.

7. The method as claimed in claim 1, further comprising the steps of:

driving an energy recovery circuit at said application time of said driving signals to raise said driving signals into a stable voltage level; and

driving the energy recovery circuit after said data was supplied to the corresponding block, thereby falling said driving signals into a ground voltage level.

8. The method as claimed in claim 7, wherein signals for driving the energy recovery circuit have a phase difference between the upper block and the lower block.

9. A driving apparatus for a plasma display panel utilizing an asymmetry sustaining wherein the plasma display panel is divided into an upper block and a lower block, said driving apparatus comprising:

a first address driver for driving first address electrode lines included in the upper block;

a second address driver for driving second address electrode lines included in the lower block; and

control means for applying first and second control signals having a desired phase difference to each of the first and second address drivers.

10. The driving apparatus as claimed in claim 9, wherein the control means includes:

controller for generating the first and second control signals and applying them to the first and second address drivers; and

a delay, being provided between the controller and the second address driver, for delaying the second control signal.

11. The driving apparatus as claimed in claim 10, wherein the delay delays the second control signal such that a driving signal can be applied from the second address driver to the address electrode lines at an approximately half time of a driving signal applied from the first address driver to the address electrode lines.

12. The driving apparatus as claimed in claim 9, further comprising:

a first scanning/sustaining driver for driving scanning/sustaining electrode lines included in the upper block;

a second scanning/sustaining driver for driving scanning/sustaining electrode lines included in the lower block; and

a common sustaining driver for driving common sustaining electrode lines included in the upper and lower blocks.